PhD thesis

<u>G. Ansaloni</u>. "*Architectural Exploration and Scheduling Methods for Coarse Grained Reconfigurable Arrays*", Università della Svizzera italiana (Lugano, Switzerland). Dissertation accepted on Setember 9th, 2011.

Peer-reviewed journal papers

2014

R. Braojos, I. Beretta, <u>G. Ansaloni</u> and D. Atienza. *"Early Classification of Pathological Heartbeats on Wireless Body Sensor Nodes",* in MPDI Sensors, vol. 14, num. 11, p. 22533-22551, 2014.

2012

<u>G. Ansaloni</u>, K. Tanimura, L. Pozzi and N. Dutt. *"Integrated Kernel Partitioning and Scheduling for Coarse-Grained Reconfigurable Arrays",* in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 31, num. 12, p. 1803-1816, 2012.

2011

<u>G. Ansaloni</u>, P. Bonzini and L. Pozzi. *"EGRA: A Coarse Grained Reconfigurable Architectural Template,"* in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, num. 6, p. 1062-1074, 2011.

Peer-reviewed conference papers

2015

S. S. Basu, P. Garcia del Valle, <u>G. Ansaloni</u> and D. Atienza. *"Significance--Based Memory Protection for Ultra--Low Power Bio-Signal Analysis Applications"*. IEEE Annual Symposium on VLSI (ISVLSI), 2015.

2014

J. Milosevic, A. Dittrich, A. Ferrante, M. Malek, D. C. Rojas Quirós R. Braojos, I. Beretta, <u>G. Ansaloni</u> and D. Atienza. *"Risk Assessment of Atrial Fibrillation: a Failure Prediction Approach"*, Computing in Cardiology (CinC), vol. 41, num. 1, p. 170-173, 2014.

H. Mamaghanian, <u>G. Ansaloni</u>, M. Sabry, D. Atienza Alonso and P. Vandergheynst. *"Hardware-Software Inexactness in Noise-aware Design of Low-Power Body Sensor Nodes*", Designing with Uncertainty - Opportunities & Challenges, 2014.

H. Mamaghanian, <u>G. Ansaloni</u>, D. Atienza Alonso and P. Vandergheynst. "*Power-Efficient Joint Compressed Sensing of Multi-Lead ECG Signals*", International Conference on Acoustics, Speech and Signal Processing (ICASSP), p. 4409-4412, 2014.

R. Braojos, H. Mamaghanian, A. Dias Junior, <u>G. Ansaloni</u>, D. Atienza, F. Rincón, and S. Murali. *"Ultra-Low Power Design of Wearable Cardiac Monitoring Systems."* Design Automation Conference (DAC), p. 1-6, 2014.

R. Braojos, I. Beretta, <u>G. Ansaloni</u> and D. Atienza. *"Hardware/Software Approach for Code Synchronization in Low-Power Multi-Core Sensor Nodes",* Design Automation and Test in Europe (DATE) Conference, p. 1-6, 2014.

F. Giroud, P. Persechini, P.-F. Ruedi, <u>G. Ansaloni</u>, R. Braojos, F. Viemon, F. Masson. *"Live demonstration: ECG sensor interface in a low power SoC for wireless portable ECG monitoring"*,

Biomedical Circuits and Systems Conference (BioCAS), p. 187-187, 2014.

2013

R. Braojos, G. Ansaloni and D. Atienza. *"A Methodology for Embedded Classification of Heartbeats Using Random Projections",* Design Automation and Test in Europe (DATE) Conference, p. 899-904, 2013.

A. Y. Dogan, R. Braojos, J. H.-F. Constantin, G. Ansaloni, A. P. Burg and D. Atienza. "Synchronizing Code Execution on Ultra-Low-Power Embedded Multi-Channel Signal Analysis Platforms", Design Automation and Test in Europe (DATE) Conference, p. 396-399, 2013.

2012

M. Milis, K. Michaelides, A. Kounoudes, G. Ansaloni, D. Atienza, F. Giroud, P. Ruedi, and F. Masson. *"IcyHeart: Highly integrated ultra-low-power SoC solution for unobtrusive and energy efficient wireless cardiac monitoring"*, IEEE International Conference on BioInformatics and BioEngineering (BIBE), p. 105-109, 2012.

R. Braojos, G. Ansaloni, D. Atienza, and F. Rincón. *"Embedded Real-Time ECG Delineation Methods: a Comparative Evaluation"*, IEEE International Conference on BioInformatics and BioEngineering (BIBE), p. 99-104, 2012.

2011

G. Ansaloni, K. Tanimura, L. Pozzi and N. Dutt. *"Slack-aware scheduling on Coarse Grained Reconfigurable Arrays"*, Design Automation and Test in Europe (DATE) Conference, p. 1-4, 2011.

2009

G. Ansaloni, P. Bonzini and L. Pozzi. "Heterogeneous coarse-grained processing elements: A template architecture for embedded processing acceleration", Design Automation and Test in Europe (DATE) Conference, p. 542-547, 2009.

2008

P. Bonzini, G. Ansaloni and L. Pozzi. *"Compiling custom instructions onto expression-grained reconfigurable architectures"*, International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES), p. 51-60, 2008.

G. Ansaloni, P. Bonzini and L. Pozzi. *"Design and Architectural Exploration of Expression-Grained Reconfigurable Arrays"*, Symposium on Application Specific Processors (SASP), p. 26 - 33, 2008.